V-Band High-Efficiency High-Power AlInAs/GaInAs/InP HEMT's

Mehran Matloubian, Linda M. Jelloian, April S. Brown, Loi D. Nguyen, Lawrence E. Larson, M. J. Delaney, Mark A. Thompson, R. A. Rhodes, and J. E. Pence

Abstract—**In this paper, we report on the state-of-the-art power performance of InP-based HEMT's at V-band. Power HEMT's were fabricated using two different material layer structures. The power performances of these HEMT's were measured at 59 GHz. We were able to achieve an output power of 155 mW with 4.9 dB gain, and power-added efficiency of 30 percent from a 448-μm-wide HEMT fabricated on a δ-doped channel layer structure. By using a double-doped layer structure, we were able to achieve an output power of 145 mW with 4.2 dB gain, and power-added efficiency of 24 percent. Output power of 288 mW with 3.6 dB gain and power-added efficiency of 20.4 percent were obtained by power combining two of the δ-doped channel HEMT's. These combinations of output power and efficiency are the best reported to date for InP-based HEMT's, and are comparable to the best results reported for AlGaAs/InGaAs on GaAs pseudomorphic HEMT's at this frequency.**

I. Introduction

INP-BASED HEMT's have demonstrated record low-noise performance at V-band [1], [2]. But little work has been done on InP-based HEMT's for power applications due to the low gate-to-drain breakdown voltage and low Schottky barrier height of these HEMT's. At V-band, the highest output power previously reported for a single AlInAs/GaInAs/InP HEMT has been 26 mW with power-added efficiency of 33 percent [3]. So far, the most promising results have been obtained on pseudomorphic AlGaAs/InGaAs on GaAs HEMT's [4]–[6]. InP-based HEMT's offer a number of advantages over GaAs-based HEMT's for power applications. The thermal conductivity of InP is 40 percent higher than GaAs, allowing a lower operating channel temperature for the same power dissipation. Due to the larger conduction band discontinuity between $Al_{0.48}In_{0.52}As$ and $Ga_{0.47}In_{0.53}As$, higher electron densities can be achieved in AlInAs/GaInAs/InP HEMT's than in AlGaAs/InGaAs/GaAs HEMT's. Coupled with the higher electron velocity in the channel, higher current densities can be achieved.

We previously reported that by proper device layer design, it is possible to overcome the drawbacks of InP-based HEMT's for power applications, and achieve power densities as high as 1 W/mm, and power-added efficiencies as high as 59 percent at 12 GHz [7]. In this paper, we report on the power performance of δ-doped channel and double-doped AlInAs/GaInAs on InP HEMT's. Using these layer structures, we have achieved state-of-the-art power performance at 59 GHz. The results are comparable to the best reported performance for AlGaAs/InGaAs on GaAs pseudomorphic HEMT's at this frequency.

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II. Device Structure

To achieve high current densities in power HEMT's without sacrificing the gate-to-drain breakdown voltage, several possible material layer structures can be used. In this study, we fabricated HEMT's using two different layer structures—a δ-doped channel layer structure and a double-doped layer structure. In a δ-doped channel layer structure (shown in Fig. 1), a plane of Si atoms is inserted at the center of the channel. In a double-doped layer structure (shown in Fig. 2), the channel is undoped and an additional donor layer is added below the channel. Both of these layers were grown by MBE on a semi-insulating InP substrate. The δ-doped layer structure consisted of a 2500 Å AlInAs buffer layer followed by a 300 Å GaInAs channel. A plane of Si atoms, with a concentration of 1.5×10^{12} cm^{-2}, was inserted at the center of this channel. In addition, a 50 Å AlInAs layer doped 6×10^{18} cm^{-3}, separated by a 15 Å undoped AlInAs spacer layer, was grown on top of the channel. To improve the Schottky barrier height of the gate, and the gate-to-drain breakdown voltage, a 250 Å undoped layer of $Al_{0.60}In_{0.40}As$ was then grown [8]. Finally, a 70 Å doped layer of GaInAs layer was grown to facilitate ohmic contact formation. The material had an electron sheet charge density of 4.2×10^{12} cm^{-2} with a mobility of 8500 $cm^2/V\text{-}s$. Even though doping the channel reduces the mobility of the electrons in the channel, it is significantly higher than the electron mobility of GaAs pseudomorphic HEMT's.

The double-doped layer structure had a δ-doped layer below the GaInAs channel with a concentration of 2.0×10^{12} cm^{-2} separated from the channel with a spacer layer thickness of 50 Å. The spacer layer was grown at significantly reduced temperatures (300–350°C) to prevent silicon movement into the channel [9]. The GaInAs channel was 200 Å thick. An additional donor layer consisting of

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$Ga_{0.47}In_{0.53}As$	CAP	70 Å
$Al_{0.60}In_{0.40}As$	SCHOTTKY	250 Å
$Al_{0.48}In_{0.52}As$	Si DOPED	50 Å
$Al_{0.48}In_{0.52}As$	SPACER	15 Å
$Ga_{0.47}In_{0.53}As$	CHANNEL	150 Å
----------		Si δ-DOPED LAYER
$Ga_{0.47}In_{0.53}As$	CHANNEL	150 Å
$Al_{0.48}In_{0.52}As$	BUFFER	2500 Å
InP SUBSTRATE		

Fig. 1. Cross section of the δ-doped channel AlInAs/GaInAs on InP power HEMT.

$Ga_{0.47}In_{0.53}As$	CAP	70 Å
$Al_{0.48}In_{0.52}As$	SCHOTTKY	100 Å
$Al_{0.60}In_{0.40}As$	SCHOTTKY	200 Å
$Al_{0.48}In_{0.52}As$	Si DOPED	50 Å
$Al_{0.48}In_{0.52}As$	SPACER	15 Å
$Ga_{0.47}In_{0.53}As$	CHANNEL	200 Å
$Al_{0.48}In_{0.52}As$	SPACER	50 Å
----------		Si δ-DOPED LAYER
$Al_{0.48}In_{0.52}As$	BUFFER	2500 Å
InP SUBSTRATE		

Fig. 2. Cross section of the double-doped AlInAs/GaInAs on InP power HEMT.

50 Å of silicon doped layer (6.5×10^{18} cm^{-3}) separated by a 15 Å spacer layer was grown on top of the channel. The Schottky layer consisted of 200 Å of undoped $Al_{0.60}In_{0.40}As$ followed by 100 Å of undoped $Al_{0.48}In_{0.52}As$, and a 70 Å $Ga_{0.47}In_{0.53}As$ layer was used as the cap. The double-doped layer structure had a sheet charge density of 4.3×10^{12} cm^{-2} with a mobility of 9800 cm^2/V-s. In both of these layer structures, electron sheet charge density in the channel is increased without increasing the doping in the top donor layer, which would result in the reduction of the gate-to-drain breakdown voltage.

HEMT's were fabricated on these two layer structures using a planar process. Source and drain ohmic contacts were formed using AuGe/Ni/Au alloy with drain-to-source spacing of 2 μm. Boron ion implantation was used for device isolation. The gates with a T-shaped cross section were formed by Ti/Pt/Au metallization with a gate length of 0.15 μm on the δ-doped channel wafer (wafer A) and a gate length of 0.2 μm on the double-doped wafer

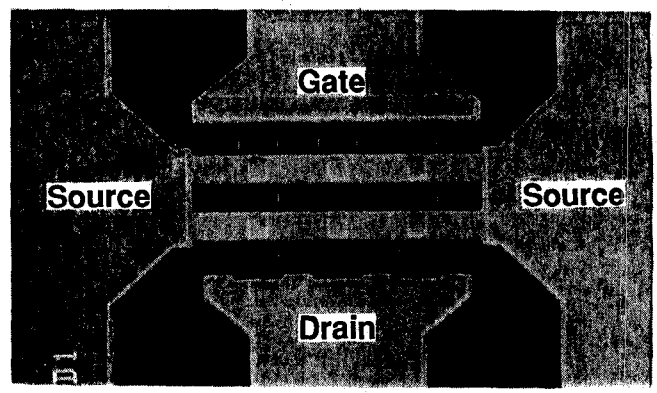

Fig. 3. SEM of 0.15 μm × 448 μm InP-based power HEMT.

(wafer B). The HEMT's had a unit gate-finger width of 56 μm and a total gate width of 448 μm with a gate-to-gate spacing of 20 μm. The picture of the device is shown in Fig. 3. The completed wafers were thinned to a thickness of 50 μm, and source vias were etched using a wet-etch process. The vias were approximately 75 μm in diameter on the back of the wafer, and 25 μm in diameter at the source pads. The back of the wafer was then metallized and plated with 8 μm of gold to add support to the wafer.

III. Device Performance

A plot of transconductance and drain current versus gate-to-source voltage for wafer A is shown in Fig. 4. The device has a peak transconductance of 600 mS/mm at a drain-to-source voltage of 1.5 V. It has a full channel current of 660 mA/mm measured at a gate-to-source voltage of 0.4 V and I_{dss} of 550 mA/mm. The gate-to-drain breakdown voltage measured at 1 mA/mm of gate current was 7 V with a gate-to-drain turn-on voltage of 0.65 V. The 448 μm HEMT's from wafer A had a current gain cutoff frequency (f_T) of 140 GHz at a V_{ds} of 1.5 V. For wafer B, the plot of transconductance and drain current is shown in Fig. 5. In this case, the device has a peak transconductance of 700 mS/mm. The full channel current is 660 mA/mm with I_{dss} of 530 mA/mm. The gate-to-drain breakdown voltage for wafer B was 6.5 V with a gate-to-drain turn-on voltage of 0.75 V. The typical f_T of 448-μm-wide HEMT's from wafer B was 120 GHz. Both of these wafers had a transconductance of more than 300 mS/mm over a drain current range of approximately 35–605 mA/mm. A summary of the dc characteristics of the two wafers is shown in Table I.

To measure the performance of the power HEMT's at 59 GHz, the devices from both wafers A and B were mounted in RF test fixtures with finline waveguide-to-microstrip transitions. The waveguide fixtures had a total loss of approximately 1.2 dB at 59 GHz, and the power measurements were corrected for this loss. The power characteristics of a 448-μm-wide HEMT from wafer A is shown in Fig. 6. The transistor was biased at a drain-to-source voltage of 3.5 V. The device has a maximum power-added efficiency of 30 percent, with an output

TABLE I
SUMMARY OF THE DC CHARACTERISTICS OF THE δ-DOPED CHANNEL AND THE DOUBLE-DOPED CHANNEL POWER HEMT'S

Wafer Profile	gm (mS/mm)	I_{df} (mA/mm)	I_{dss} (mA/mm)	BV_{gd} (V)	V_{gd} (V) (turn-on)	$V_{\text{pinch-off}}$ (V)
delta-doped	600	660	550	7	0.65	−1.2
double-doped	700	660	530	6.5	0.75	−1

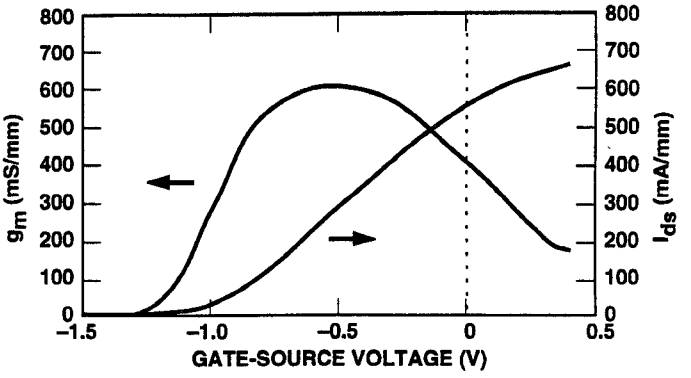

Fig. 4. Plot of transconductance and drain current as a function of gate-to-source bias at V_{ds} = 1.5 V for the δ-doped channel wafer (wafer A).

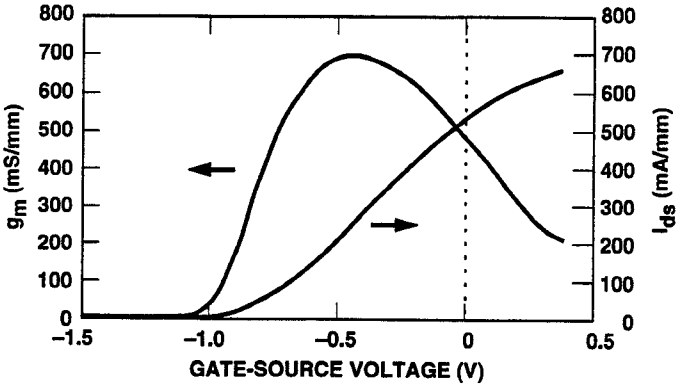

Fig. 5. Plot of transconductance and drain current as a function of gate-to-source bias at V_{ds} = 1.5 V for the double-doped wafer (wafer B).

power of 155 mW and 4.9 dB gain. The transistor has a linear gain of 8 dB and a saturated output power of more than 180 mW with a 3 dB gain. The 448-μm-wide HEMT from wafer B was also biased at a drain-to-source voltage of 3.5 V. The device had a maximum power-added efficiency of 24 percent, with an output power of 145 mW and 4.2 dB gain. The linear gain for this device was approximately 7 dB. Table II shows a summary of the power performance of devices from these two wafers.

To achieve higher output powers at 59 GHz, branch-line couplers fabricated on alumina substrates were used to power combine two 448-μm-wide HEMT's from wafer A. Fig. 7 shows the power characteristics of the two devices combined. The discontinuity in the output power is due to retuning of the amplifiers at that input power level. The output power at the maximum power-added efficiency of 20.4 percent is 288 mW with a gain of 3.6 dB. The combiner has an output power of more than 320 mW

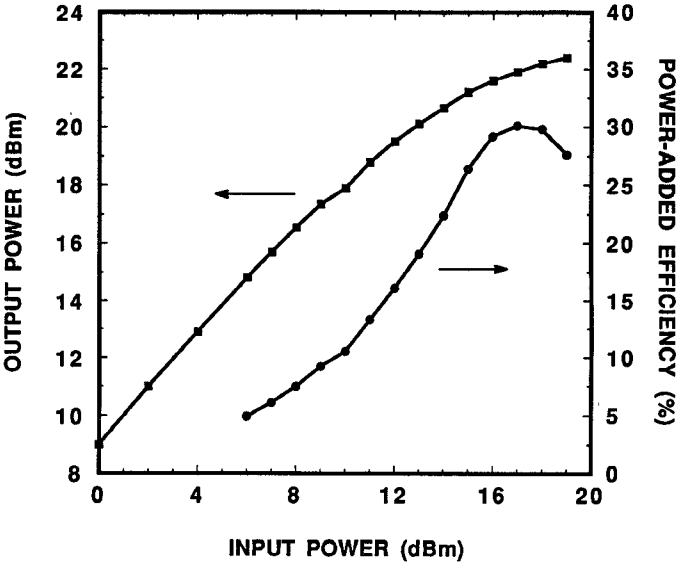

Fig. 6. Power characteristics of a 448-μm-wide δ-doped channel HEMT at 59 GHz.

TABLE II
SUMMARY OF THE POWER PERFORMANCE OF THE δ-DOPED CHANNEL AND THE DOUBLE-DOPED CHANNEL POWER HEMT'S

Wafer	Output Power (mW)	Power-Added Efficiency (%)	Power Gain (dB)	Linear Gain (dB)
delta-doped	155	30	4.9	8
double-doped	145	24	4.2	7

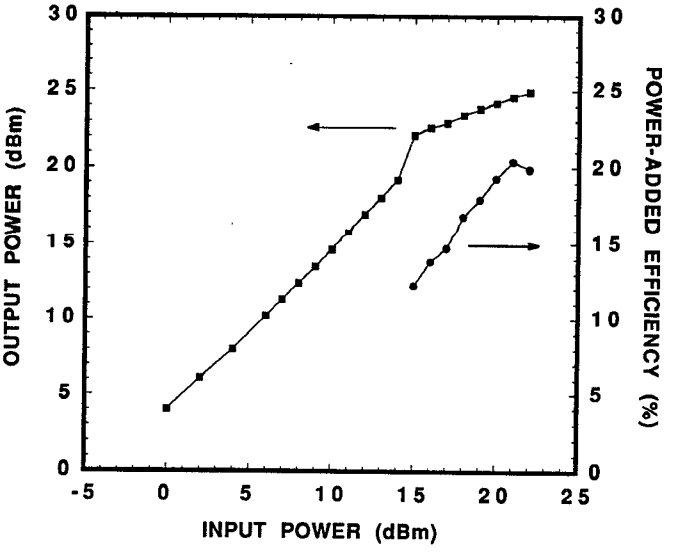

Fig. 7. Power characteristics of power combined two 448-μm-wide δ-doped channel HEMT's at 59 GHz.

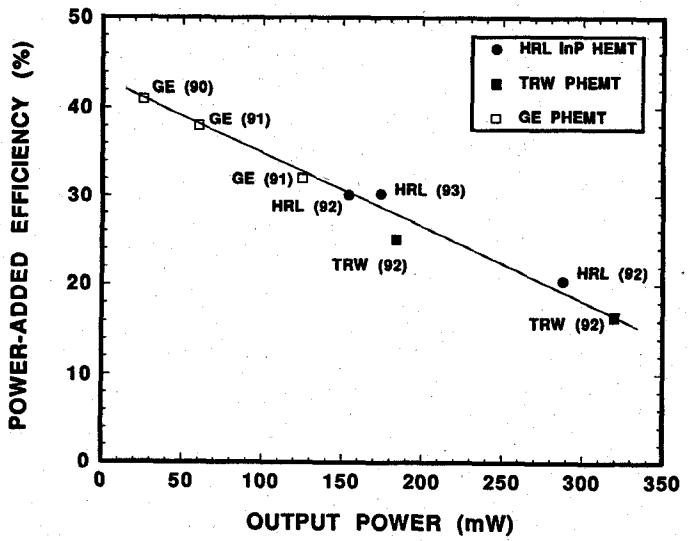

Fig. 8. Comparison of the-state-of-art power performance for HEMT's at about 60 GHz.

with power-added efficiency of 19 percent. A comparison of state-of-the-art power performance for HEMT's at 60 GHz is shown in Fig. 8. As can be seen from a comparison of output power and power-added efficiency, the data presented in this paper on AlInAs/GaInAs/InP HEMT's are comparable to the best results reported on AlGaAs/InGaAs/GaAs PHEMT's.

IV. Conclusion

In this paper, we compared two possible layer structures for fabrication of V-band power HEMT's and reported the first V-band power results of a double-doped AlInAs/GaInAs on InP HEMT. We were able to achieve an output power of 155 mW with power-added efficiency of 30 percent and 4.9 dB gain from a δ-doped layer structure, and an output power of 145 mW with 4.2 dB gain and power-added efficiency of 24 percent from a double-doped layer structure. The lower gain and efficiency of the double-doped layer structure are believed to be due to the slightly longer gate length of the devices from that wafer. Using a gate length of 0.15 μm with the double-doped layer structure should increase the gain, and therefore the power-added efficiency of the transistor. Recently, we have demonstrated device yield of more than 90 percent for 50-μm-wide low-noise InP-based HEMT's with gate length of 0.1 μm [10]. By further optimization of the material layer structure, and by incorporating a 0.1 μm gate in our power HEMT's, we expect improvements in V-band power performance of the transistors.

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During the academic year of 1985–1986, she taught at the University of Michigan, Ann Arbor, as an Assistant Professor. In 1986 she joined Hughes Research Laboratories, Malibu, CA, as a Member of the Technical Staff and was responsible for the pioneering development of InP-based HEMT materials and devices at Hughes. She temporarily left Hughes for the Army Research Office from 1988 to 1989, where she monitored programs in condensed matter physics. She rejoined Hughes in 1989. She is currently a Senior Scientist and is responsible for the growth and characterization of InP-based HEMT materials, the development of an InP-based power HEMT, as well as the exploration of novel materials and growth mechanisms.

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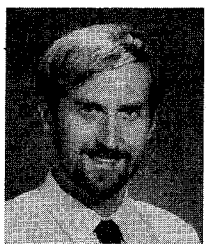
He has made significant contributions to the design, fabrication, and modeling of ultrashort gatelength High Electron Mobility Transistors (HEMT's). He is currently a Department Manager at Hughes Research Laboratories in Malibu, CA, and is responsible for the pilot line production of high-reliability, ultralow-noise InP-based HEMT's and their associated monolithic circuits for radars and satellite communications. His research interests concentrate on the design, fabrication, characterization, and modeling of ultrashort gatelength HEMT's, as well as the development of new and novel compound semiconductor materials and devices. He has written or contributed to approximately 30 publications.



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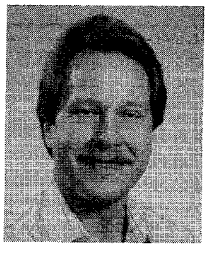

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R. A. Rhodes, photograph and biography not available at the time of publication.

J. E. Pence, photograph and biography not available at the time of publication.